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Step Free Surface Heteroepitaxy of 3C-SiC Layers on Patterned 4H/6H-SiC Mesas and Cantilevers

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Abstract. The *off-axis* approach to SiC epitaxial growth has not prevented many substrate crystal defects from propagating into SiC epilayers, and does not permit the realization of SiC heteropolytype devices. This paper reviews recent advancements in SiC epitaxial growth that begin to overcome the above shortcomings for arrays of device-sized mesas patterned into *on-axis* 4H/6H-SiC wafers. These on-axis mesa growth techniques have produced 4H/6H-SiC homoepilayers and 3C-SiC heteroepilayers with substantially lower dislocation densities. The results should enable improved homojunction and heterojunction silicon carbide prototype devices.

Introduction

Presently, almost all SiC devices are implemented in homoepitaxial films of the 4H/6H-SiC polytypes grown on commercial SiC wafers with surfaces polished 3° to 8° off the (0001) basal plane [1]. Homoepitaxy of 4H/6H-SiC, including growth performed on non-standard $(11\bar{2}0)$ and $(03\bar{3}8)$ surfaces, is kinetically controlled growth, in that it relies on lateral bilayer expansion from substrate step edges for growth and structural stacking sequence replication [2, 3]. While these epitaxial growth processes have achieved some useful alterations of dislocation character, such as dissociation of micropipe defects, these methods nevertheless do not eliminate the majority of dislocations found in SiC substrates from SiC epilayers [1, 4, 5]. For example, the basal-plane expansion of stacking fault defects through off-axis homoepilayers has prevented the commercialization of high-voltage SiC bipolar power devices [6]. The properties of off-axis 4H/6H-SiC epilayer-oxide interfaces have also proven insufficient for commercialization of inversion-channel SiC MOSFET's [7]. Furthermore, the kinetically controlled off-axis growth approach does not permit controlled realization of SiC heteropolytype junctions and devices. The inability to surmount these fundamental issues has (to date) precluded the most successful device topologies in semiconductor electronics (i.e., the inversion-channel MOSFET, bipolar power device, and heterojunction transistor) from being commercialized in SiC.

This article briefly reviews and updates recent advancements in SiC epitaxial growth that begin to overcome the above shortcomings when implemented on arrays of mesas patterned into commercial nearly *on-axis* SiC wafers. These advancements are largely based upon properly controlling the SiC growth surface step structure to a degree not possible with off-axis wafer polish. These techniques have produced improved-quality 4H/6H-SiC and heteroepitaxial 3C-SiC that should enable a variety of improved homojunction and heterojunction silicon carbide electronic devices. Additional experimental information is available in the cited references.

On-Axis Epitaxial Growth of Step-Free (0001) SiC Mesa Surfaces

On-axis Homoepitaxy. When step-controlled SiC epitaxy was introduced, it was originally thought that high surface miscut angles (i.e., > 1° "off-axis" from the (0001) basal plane yielding a growth surface with high bilayer step density and short terrace widths) were necessary for homoepitaxy of SiC to occur at temperatures below 1600 °C [3, 8]. However, Powell et al. pioneered "on-axis" (i.e., < 0.5° surface polish error from the basal plane) homoepitaxial growth of 6H-SiC over large (several mm) areas at 1450 °C by employing an in-situ 1375 °C HCl/H_2 etch prior to the initiation of epitaxial growth [9]. To explain the results, Powell proposed a growth model wherein previously observed terrace nucleation of 3C-SiC was facilitated by dislocations and surface contamination, and not a result of insufficient surface mobility of precursor adatoms. Powell's crucial findings are strongly supported by additional work at NASA ([10-13] summarized below), and subsequently have been further verified by more recent on-axis growth results reported by Kyoto University [14-16].

Step-Free Mesa Formation. The ability to suppress 2D nucleation of 3C-SiC on large (hundreds of μm) basal plane terraces while carrying out stepflow homoepitaxy led to the development of device-sized 4H/6H-SiC mesa regions with top surfaces completely free of organized atomic-scale steps. The process is illustrated in the simplified schematic cross-sections of Fig. 1a-b [10, 13, 17]. Trenches are etched into the 4H/6H-SiC on-axis wafer surface (Fig. 1a). Following an in-situ H_2 or HCl/H_2 etch, pure stepflow homoepitaxy (2D nucleation suppressed) grows all initial surface steps over to the edge of the mesa. This leaves behind a step-free (0001) basal plane as the top surface of a 4H/6H homoepilayer with wedge-like thickness profile ("epi-wedge", Fig. 1b). The results imply that additional 4H/6H-SiC bilayers cannot be added to an existing (0001) terrace without screw dislocations (SD's) that provide a polytype template and new growth steps. Where SD's are present, on-axis homoepitaxial growth of 4H/6H-SiC can be carried out with tenth-degree surface miscut angles [10, 13].

Homoepitaxial Cantilevers. As illustrated in Fig. 1c, continued epitaxial growth of a screw-dislocation-free 4H/6H-SiC mesa leads to the formation of thin lateral cantilevers that extend the step-free surface area from the top edge of the mesa sidewalls [11-13]. With terrace nucleation suppressed, growth adatoms harvested by the step-free surface migrate to the mesa edges where the more favorable sidewall bonding leads to incorporation into the crystal near the top of the mesa sidewall. By selecting a proper pre-growth mesa shape and crystallographic orientation, the rate

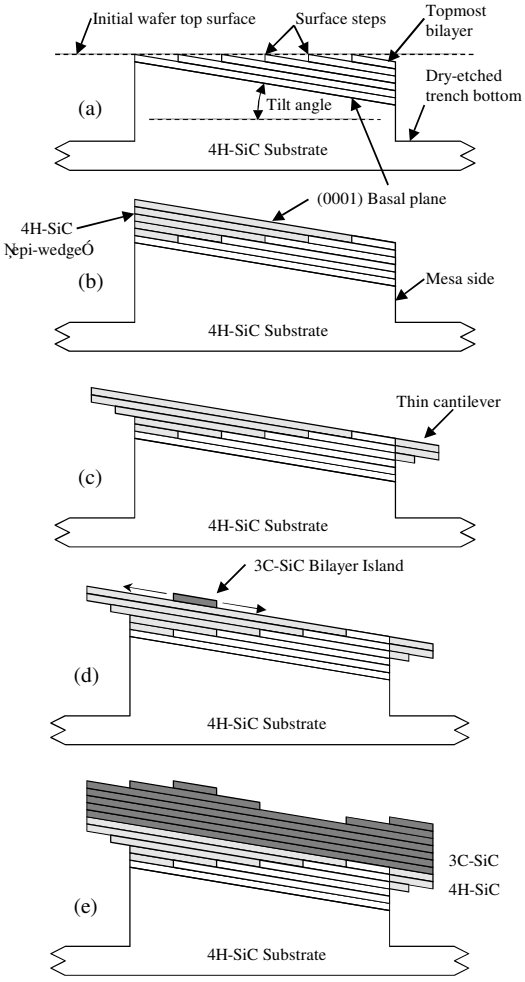

Fig. 1. Simplified cross-sectional depictions (showing bilayer planes) of on-axis SiC mesa growth processes: (a) 4H-SiC mesa prior to growth. (b) Pure stepflow growth to produce step-free 4H-SiC mesa surface. (c) Extension of step-free surface by cantilever growth. (d) Initiation of 3C-SiC heterofilm by intentional terrace nucleation and lateral expansion of 3C bilayer island. (e) continued growth of 3C-SiC film.

of cantilever growth can be greatly enhanced in a "web growth" process [11-13].

Reduction/Relocation of Dislocations. Due to the fact that the crystal structure of the thin SiC cantilevers is established laterally from mesa sidewalls, these cantilevers have demonstrated the ability to overgrow, relocate, and consolidate dislocations (including micropipes) residing in the substrate [11-13, 18]. Using pre-growth mesa patterns to promote thin cantilevers that progressively coalesce outwardly on a non-enclosed mesa shape (such as the open "V-shaped" mesa of Fig. 2a), device-sized webbed cantilever surfaces *completely free of defects* were realized, even when the webbing resided directly over substrate micropipes [11, 12]. In particular, *KOH etching failed to produce any hexagonal etch pits in outwardly-coalesced 4H-SiC cantilevers* [18]. However, small etch pits (not related to SD's) are observed in pre-growth mesa regions that support the thin lateral webbing (Fig. 2a etch pit) and when webbed regions coalesced down to an interior point (pit P2 in Fig. 2b). Fig. 2b shows KOH etch pit defects observed when thin webbed cantilevers from multiple mesa sides converge to completely roof six triangular hollow trench regions enclosed by the support mesa. Larger KOH etch pits S1, S2, and S3 shown in Fig. 2b correspond to elementary SD's formed at the final points of cantilever coalescence [13, 18]. Smaller KOH etch pits P1-P4 are consistent with epilayer threading edge dislocations [19].

Based upon the principle of Burgers vector conservation, we hypothesize that all c-axis propagating substrate dislocations enclosed by a given hollow region become combined into a single dislocation in the webbed film roof at the point of final roof coalescence. The point of final roof coalescence, and therefore the lateral location of a webbed roof dislocation, can be designed into the pre-growth mesa pattern. SD's with predetermined lateral position can then be used to provide new growth steps necessary for growth of a 4H/6H-SiC epilayer with lower dislocation density than the substrate. Devices fabricated on top of such films can then be patterned to avoid pre-placed dislocations [13, 18].

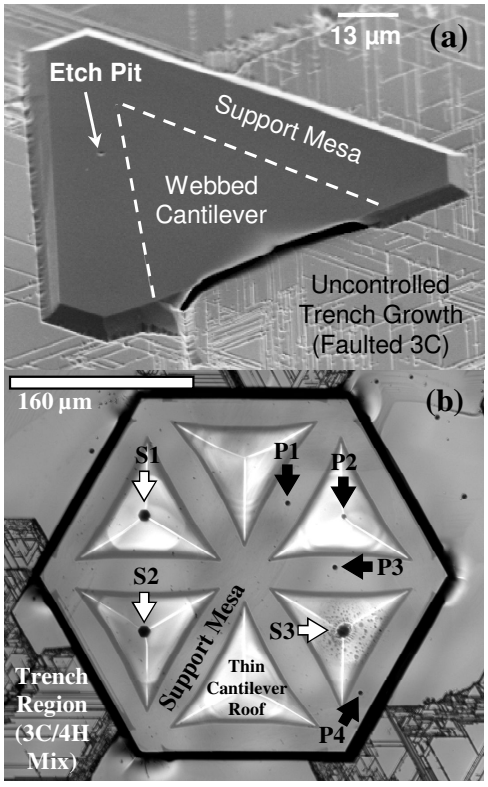

Fig. 2. KOH etch pits on lateral webbed cantilevers grown from (a) open "V-shaped" support mesa and (b) "spoked-hexagon" support mesa with six hollow triangular regions. No etch pits are observed on properly coalesced cantilevers (such as (a)).

Heteroepitaxial Growth of 3C-SiC.

3C-SiC Film Nucleation. Once homoepitaxial growth has achieved step-free mesas (with or without cantilevers), heteroepitaxial nucleation of 3C-SiC can be initiated on the step-free 4H/6H-SiC surface in a controlled manner [13, 20]. We have named this process "step-free surface heteroepitaxy", as this reflects the nature of the 4H/6H growth surface prior to 3C growth initiation. Most often, intentional terrace nucleation of 3C-SiC on the step-free 4H/6H surface has been induced by ramping the temperature downward without any growth interruption from the ~ 1600 °C temperature used to grow the step-free 4H/6H mesa surfaces. The decreased growth temperature decreases surface adatom mobility, thereby increasing the probability of 2D nucleation that initiates 3C-SiC growth (Fig. 1d).

In the absence of kinetic step-flow polytype control, our experimental results indicate that there is a strong thermodynamic driving force for new bilayers to continue the local cubic stacking of the immediately underlying two bilayers [13, 17]. Therefore, the use of a step-free surface effectively eliminates double positioning boundary (DPB) epilayer defects that could otherwise occur when opposite rotations of 3C-SiC nucleate on a stepped surface and subsequently coalesce [3, 8, 13, 17, 20]. For step-free 4H/6H mesas, the stacking fault (SF) content of 3C-SiC mesa films varied significantly as a function of 3C growth initiation process. 3C-SiC mesa heterofilms nucleated more slowly using gradual temperature ramp decreases exhibited higher SF-free yields than films nucleated with rapid temperature ramp decreases [13, 20]. We proposed a growth model in which the low initial nucleation rate enables 3C-SiC heteroepitaxial growth to initiate from a single 3C-SiC island, thereby eliminating SF-defects associated with coalescence of multiple 3C-SiC islands expanding laterally on a step-free 4H-SiC mesa. We have theorized that the driving force for the defective 3C island coalescence leading to SF formation is in-plane lattice mismatch between the 3C-SiC film and the step-free 4H/6H mesa [20-23].

Initial characterization of unintentionally doped 3C-SiC mesa heterofilms below 4 μm thick by thermal oxidation, scanning electron microscopy (SEM), X-ray topography, high resolution X-ray diffraction (HRXRD), cross-sectional tunneling electron microscopy (XTEM), and molten KOH etching has been previously reported [13, 20-25]. While these results have been largely consistent with the growth model described above, further experiments are required for more complete understanding of all aspects of the 3C-SiC heterofilm growth. Towards this end, some recent new experimental findings are summarized below.

Heterofilm Etch Pit Defects. Recent experimental data that indicates that the majority of isolated 3C-SiC heterofilm etch pits reported in [25] for SF-free mesas originate from defects in the underlying 4H-SiC substrate. Molten KOH etching was performed on thin 3C-SiC mesa films. In some sample regions the 3C-SiC was thin enough that etch pits penetrated the 4H/3C interface. Fig. 3 shows a typical example of a "through 3C film" etch pit found on SF-free 3C mesas, compared to homogeneous 3C (top inset) and 4H (bottom inset) etch pits. The top portion of the mixed etch pit has partial triangular 3C character, while the deeper portion of the pit exhibits pointed-bottom hexagonal facet geometry consistent with previously reported 4H-SiC dislocation pits [19, 25]. This pit geometry indicates that preferential etching below the thin 3C-SiC layer is enabled by a dislocation defect extending into the 4H-SiC. If no dislocation were present in the 4H-SiC, the lack of preferential etching below the 3C/4H interface should have produced flat-bottomed pit geometry. To date, all pits etched through thin 3C films exhibit pointed-hex-bottom geometry similar to Fig. 3.

The etch pit observations correlate isolated 3C etch pits observed in thin SF-free 3C heterofilms to dislocation defects residing in the underlying 4H-SiC mesa. Given the propagation of 4H-SiC dislocations reported by Ha et al [19], it is likely that threading edge dislocations (propagating through the Fig. 1b 4H "epi-wedge") are the 4H-SiC defect responsible for 3C pit formation. Therefore, we hypothesize that most isolated 3C-SiC etch pits observed on SF-free mesas are due to 3C edge dislocations that originate from edge dislocations in 4H-SiC homoepilayer. Because properly webbed 4H/6H-SiC cantilevers (such as Fig. 2a webbed cantilever) do not exhibit any etch pits, we believe that growth of 3C-SiC films on webbed surfaces should eliminate most isolated pit defects in SF-free 3C-films.

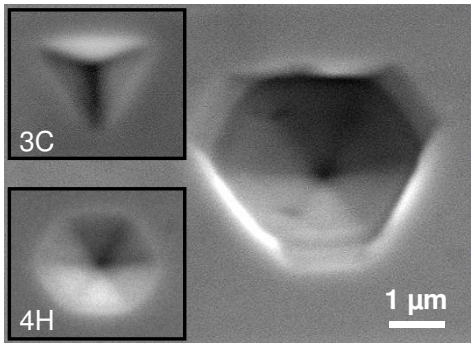

Fig. 3. KOH etch pit (right) formed from a dislocation propagating from 4H mesa into thin 3C layer.

Thick 3C-SiC Films. After an initial thickness of 3C-SiC film has been properly nucleated and grown on top of the 4H/6H mesa surface, growth of additional 3C-SiC crystal can be viewed somewhat as being a homoepitaxial

growth process. Because 2D nucleation of new crystal bilayers thermodynamically continues the cubic stacking of immediately underlying bilayers [13, 17, 24], additional growth of 3C-SiC epilayers can be accomplished over a wider range of epitaxial process conditions than is possible with 4H/6H homoepitaxy that demands stepflow without terrace nucleation. This fundamental process advantage also applies to the potential realization of high-quality bulk 3C-SiC crystals, which could theoretically be enlarged from small seed crystals without excessive temperatures and screw dislocations required for bulk growth of 4H/6H boules [1]. Fig. 4 shows an SEM of two unintentionally doped 3C mesa films in excess of 13 μm thick that were grown for 4 hours at ~1550 °C on SD-free hexagon-shaped 4H-SiC mesas [26]. The density of both SF's and molten KOH etch pits for the thick 3C mesa films were (to within experimental error) not greater than those obtained on thin 3C-SiC films. The sides of the Fig. 4 thick mesa films exhibit some faceting similar to previous 3C observations [27].

AFM studies of 3C mesas grown at temperatures from ~ 1300 °C to ~ 1700 °C show the 3C film surfaces to be dominated by 0.25 nm height (i.e., single Si-C bilayer thickness) steps. Macrostep formation (i.e., step bunching) is almost never observed in SF-free 3C mesa films. The observed 3C mesa film morphology and growth rate as a function of dislocation defect content and growth temperature are presented elsewhere at this conference [26].

Doping of 3C-SiC Device Films. Controlled doping of 3C mesa heteroepilayers is necessary to realize prototype 3C-SiC devices. Using site-competition, aluminum doping of a 3C-SiC mesa film was varied from 10^{16} to 10^{20} cm^{-3} while maintaining a better than 50% yield of 3C mesas entirely free of SF's and DPB's [28]. However, these films were unintentionally contaminated by ~ 10^{17} cm^{-3} boron. 3C-SiC Schottky diodes fabricated on these films showed excellent reverse blocking characteristics, exhibiting breakdown fields in excess of 2 MV/cm for 1-5x10^{17} cm^{-3} boron doping [29]. Nitrogen doping experiments are in progress.

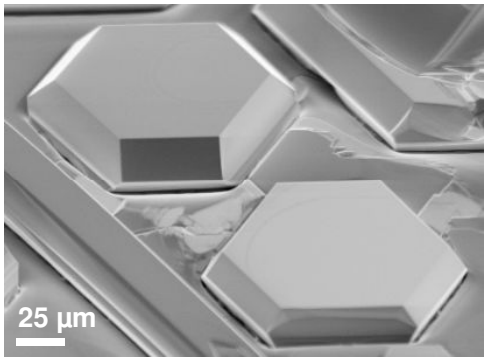

Fig. 4. Thick (> 13 μm) SF-free 3C-SiC mesa films grown on top of hexagon-shaped 4H-SiC mesas.

Discussion

In contrast to off-axis growth approaches, the on-axis mesa growth techniques described above have demonstrated the ability to reduce and relocate dislocations in patterned SiC epilayer regions. An intrinsic character of on-axis growth is that dislocations confined to the basal plane will not propagate through an epilayer thickness. The mesa approach offers a growth platform free of damaging stresses imposed by growth through patterned masking materials. Improved mesa crystals are of sufficient size to begin implementing prototype on-axis SiC devices for fundamental comparisons (more completely described in [13]) to 4H/6H off-axis device approaches. For example, experimental bipolar power devices implemented in nearly dislocation-free on-axis 4H/6H-SiC or 3C-SiC mesa epilayers might avoid forward bias degradation (bias/stress-driven transformation towards more cubic stacking) that has plagued off-axis 4H/6H-SiC power diodes [6]. Fault-free 3C-SiC can be tested as a unique platform for realizing SiC MOSFET's with both higher mobility and higher oxide reliability than achieved with unfavorable 4H/6H-SiC oxide interface properties [7]. The controlled manner in which 3C-SiC is intentionally nucleated on a step-free 4H/6H surface should facilitate abrupt interfacial doping needed to realize 3C/4H heterojunction transistors.

The primary size limitation of step-free mesa growth to date has been that atomic flattening and cantilevering cannot be achieved when a pre-growth mesa contains a substrate screw dislocation [10, 12, 13]. Experiments aimed at growing larger mesa epilayers with lower etch pit density are planned. However, the difficult crystal growth challenge of scale-up to bulk wafer size is only likely to be undertaken if small-area prototype device experiments convincingly demonstrate significantly superior on-axis SiC device performance not attainable with other SiC growth approaches.

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